REMARKS

This responds to the Final Office Action mailed on September 9, 2005, and the references cited therewith.

Claims 9 and 15 have been amended to more particularly point out the claimed invention. Claims 1 – 26 are now pending in this application. No new matter is added by these amendments.

For the reasons discussed below, Applicants submit that the above amendments clearly place the claims in condition for allowance and do not add new matter or require further consideration and/or search. Accordingly, Applicants respectfully request entry of the amendment pursuant to 37 C.F.R. 1.116.

Objections

Claim 9 was objected to under 37 C.F.R. 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicants amended claim 9 to depend on independent claim 1. Accordingly, Applicants request that the objection to be withdrawn.

Claim Rejections – 35 U.S.C. §103

Claims 1-26 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Miyazawa (U.S. Patent No. 5,907,682; hereinafter "Miyazawa") in view of Wolf et al. (U.S. Patent No. 6,526,069; hereinafter "Wolf"). Applicants respectfully traverse these rejections.

Of the rejected claims, claims 1, 10, 14, 15, 17, 18 and 20 are independent claims and claims 2 – 9, 11 – 13, 16, 19 and 21 – 26 are dependent claims. Miyazawa and Wolf, taken singly or in combination, all fail to teach, suggest, or disclose all of the limitations of claim 1:

> a temporary storage device, comprising:
>
> a first buffer, the first buffer configured to receive information, the information provided in association with a line clock signal, the first buffer configured to receive a first write enable signal for storing a first portion of the information;
>
> a second buffer, the second buffer configured to receive the information, the information provided in association with the line clock signal, the second buffer

configured to receive a second write enable signal for storing a second portion of the information different from the first portion of the information;

a **system clock** signal provided to the first buffer and the second buffer for **synchronously clocking** out the first portion and the second portion of the information; and

a pointer processor coupled to the first buffer to receive the first portion of the information, the pointer processor have a third buffer for storing the first portion of the information.

Emphasis Added. Applicants' invention of claim 1 provides an apparatus for reducing misalignment of pointer output owing to misalignment of clock signal edges. *Specification*, Page 2, paragraph 14. A system clock signal, such as a drop clock signal 13, is provided in part to buffers 130 and 140. *Specification*, Page 4, paragraph 49. These buffers are synchronously operated on an output side off a **system clock signal**. *Emphasis Added. Specification*, Page 4, paragraph 50. Referring to Applicant's Figure 2B, after inputting frame structure into buffer, information from such frame structure is synchronously clocked out of buffer using a system clock signal. *Specification*, Page 5, paragraph 52.

The Examiner relies on Wolf as teaching a system clock signal provided to the first buffer and the second buffer for synchronously clocking out the first portion and the second portion of the information. In order to establish a prima facie case of obviousness, the prior art must teach all of the claimed limitations and must provide a motivation for any combination of teaching from multiple references. Here, Applicants submit that at least Miyazawa cannot be properly combined with Wolf.

Miyazawa discloses a communication LSI for executing protocol processes of a transmission frame with a physical layer. *Miyazawa*, Col. 4, lines 7 – 12; Col. 8, lines 27 – 30. One of the objects of the invention is to **reduce the scale** of the communication LSI hardware. *Emphasis Added. Miyazawa*, Col. 8, lines 27 – 32. The reception system of the physical layer LSI contained a disassembling section 100. *Miyazawa*, Col. 5, lines 21 – 33. The disassembling section 100 comprises **a frame synchronization circuit** 100-1 for executing synchronization operation based on data received from the network system of the physical layer LSI. *Emphasis Added. Miyazawa*, Col. 5, lines 21 – 33; Figure 5. The frame synchronization circuit executes synchronization operation by detecting synchronization words at the head of the reception frame. *Miyazawa*, Col. 5, lines 40 – 42. A frame counter executes a count operation in synchronization

with the reception frame under control of the frame synchronization circuit. *Miyazawa*, Col. 5, lines 42 – 45.

The Examiner concedes that Miyazawa fails to disclose the use of a system clock signal to synchronously clock out data stored in the buffers. The Examiner points to Wolf for disclosing a system clock signal to the first buffer and the second buffer for synchronously clocking out the first portion and the second portion of the information. However, Wolf does not disclose such a limitation. Rather Wolf discloses a synchronization device and process for a synchronous digital message transmission system. *Wolf*, Col. 1, lines 9 – 14. The system produces a synchronous output signal out of a digital input signal. *Wolf*, Col. 1, lines 9 – 14. The synchronization device includes, in relevant part, a **write clock WCLK and a read clock RCLK**. *Emphasis Added. Wolf*, Col. 3, lines 30 – 33; Figure 2. Synchronous operation is performed by **synchronizing the read clock to the reference clock** pulse of the message transmission system. *Emphasis Added. Wolf*, Col. 3, lines 40 – 45.

To merely apply the system clock in Wolf into a communication LSI of Miyazawa may increase the complexity of the communication LSI hardware. Thus Miyazawa fails to disclose the use of a system clock signal to synchronously clock out data stored in the buffers. Moreover, Miyazawa teaches away from using system clock signal to synchronously clock out information stored in the buffers by utilizing **a frame synchronization circuit** based on data received from the network system of the physical layer. *Emphasis Added.* As a result, no particular synchronization signal is required. *Miyazawa*, Col. 8, lines 55 – 65.

Therefore, the proposed modification of Miyazawa with the teachings of Wolf would render the system of Miyazawa unsatisfactory for its intended purpose, and therefore, would not have been obvious. *See* MPEP 2143.01. In rendering the proposed modification of Miyazawa unsatisfactory for its intended purpose, Wolf cannot be considered as suggesting a motivation to combine the teachings of the references or any modification of the teachings.

Independent claims 10, 14, 15, 17, 18 and 20 each require similar limitations as discussed above in claim 1 and thus, Applicants respectfully submit claims 10, 14, 15, 17, 18 and 20 are also allowable over Miyazawa and Wolf. Applicants respectfully submit that dependent claims 2 – 9, 11 – 13, 16, 19 and 21 – 26 are also allowable by virtue of their dependency from the independent claims in addition to their own further limitations.

Conclusion

Having dealt with all the objections and/or rejections raised by the Examiner, it is respectfully submitted that the present application, as amended, is in condition for allowance. Thus, allowance is earnestly solicited.

If the Examiner desires personal contact for further disposition of this case, the Examiner is invited to call the undersigned Attorney at 603-668-6560. In the event there are any fees due, please charge them to our Deposit Account No. 50-2121.

Respectfully submitted,

Ang et al.

By their Representatives,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 9 day of November, 2005.

Chris Hammond _____

Name Signature